REMARKS

Claims 1, 3, 5-10, 12, and 14-19 are all the claims presently pending in the application. Claims 1 and 8 have been amended to more clearly define the invention and claims 18-19 have been added. Claims 14-17 have been withdrawn from prosecution. Of the remaining claims, claim 1 is independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, Applicant's intent is to encompass equivalents of all claim elements.

Claims 1, 3, 5-10, and 12 continue to stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Takao, et al. reference in view of the Bemis reference.

This rejection is respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

An exemplary embodiment of the claimed invention, as recited by independent claim 1, is directed to a magnetic disk apparatus which includes a plurality of disk enclosures, a plurality of first printed-circuit boards which are paired with the disk enclosures, and a second printed-circuit board which is detachably connected to the first printed-circuit board via a cable. The first printed-circuit boards mount circuits which have a first noise resistance property, and a circuit which holds parameters unique to the disk enclosure. The second printed-circuit board mounts circuits which have a second noise resistance property which is superior to the first noise resistance property. The second printed circuit board is also

detachably connectable to an upper system. The circuits on each of the plurality of first printed-circuit boards include a recording/reproduction control circuit.

Conventional magnetic disk apparatus have only a single printed-circuit board for a single disk enclosure. Such single printed-circuit boards mount all of the circuits for controlling the disk enclosure. Thus, when the disk enclosure is exchanged for another disk enclosure, all of the circuits for each disk enclosure must also be exchanged because all of the circuits are on the same single printed-circuit board as the disk. This leads to a wasted cost in replacing all of the circuits for each disk enclosure and maintains a high cost for such a disk exchange. It also limits miniaturization of such a disk enclosure

By contrast, the present invention provides a disk apparatus which includes two separate printed-circuit boards. A plurality of first printed-circuit boards (e.g., 21 and/or 22 in the exemplary non-limiting embodiment of Fig.2) includes the disk enclosure and is only required to also include those circuits which are unique to the disk enclosure (e.g., such as the exemplary parameter holding circuit 4 in Fig. 1). A second printed-circuit board (e.g., 23 in the exemplary non-limiting embodiment of Fig. 2) includes other circuits. Thus, when the disk enclosure requires an exchange with another disk enclosure, only those circuits on the first printed-circuit board are exchanged, thereby significantly reducing the cost of the exchange.

Additionally, the exemplary embodiment of the present invention includes a recording/reproduction control circuit on the first printed-circuit board. The recording/reproduction control circuit inputs and outputs high-frequency signals in order to control the circuit in the first circuit board such as the analog/digital converter.

If the recording/reproduction control circuit is placed in the second printed circuit

board, then lines for the high-frequency signals become long to extend from the second printed circuit board to the first printed circuit board, whereby the high frequency signals in the long line strongly interfere with the recording signal, the reproduced signal and other signals, which may cause errors of the recording signal, errors of the reproduced signal and defective operation in the circuits of the first printed circuit board.

Further, if the recording/reproduction control circuit is placed in the second printed circuit board, then the high frequency is delayed due to capacitance between the long lines and ground. The phase delay of the high frequency is proportional to the frequency, and the phase delay causes a defective timing sequence for reading and writing data.

Therefore, it is effective to place the recording/reproduction control circuit in the first printed circuit board.

II. THE PRIOR ART REJECTION

The Examiner alleges that the Bemis reference would have been combined with the Takao et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Regarding claim 1, the Bemis reference discloses that the circuit 400 includes a switch for selecting either one of a plurality of drives A to F. However, each of drives A to F is a conventional device which corresponds to disk enclosure 82 as shown in Figure 5 of the present application.

The Bemis reference appears to disclose drives A to F which constitutes a RAID (Redundant Array of Inexpensive Disks) (Figures 6 and 7 illustrate the use of the spare disk

drive within the RAID level 3 disk array shown in Figure 1 (col. 7, lines 63-63)) and that in a personal computer, a RAID system is constructed by using a RAID PCI board or a RAID chip on a mother board and a plurality of IDE hard drives, disk enclosures.

In stark contrast, in accordance with the present invention, the switch included in the second printed-circuit board selects either one of the plurality of first printed-circuit boards connected to the second printed-circuit board and another of the plurality of first printed-circuit boards connected to the second printed-circuit board. The first printed-circuit board and the second printed-circuit board constitute convention disk enclosures. That is, the first printed-circuit board is a part of the conventional disk enclosure.

Therefore, the switch that is disclosed by the Bemis reference does not correspond to the switch that is recited by claim 1 because the targets are different.

Regarding claim 3, the Takao et al. reference discloses:

> "[0038] Data signals, such as a text file sent from the information machines and equipment circuit 4 by interface bus methods, such as SCSI and PC/AT, - - - HDC (hard disk controller) 63 within an interface 5 - - a passage - - once - - RAM (random access memory:rewriteable storage element) 64 - - storing - - - having. HDC63 performs bus control and an error correction. The data stored in RAM64 are transmitted to GA (gate array) 65 by directions of the microcomputer 61 of a logic operation circuit 6, and are changed into the code sequence suitable for magnetic recording. The code sequence changed by GA 65 is changed into the data wave which is suitable for magnetic recording in the channel circuit 66, and is sent to the R/W amplifier 7 arranged in the 1st case 2a. Whether magnetic recording is written to the field of

magnetic disck 11 passes the current according to a wave from the R/W amplifier 7 to the magnetic head 13 according to a head selection signal, and magnetic recording is performed."

"[0039] Thus, as the data recorded on the magnetic disk 11 are the following conversely, they are sent to the information machines and equipment circuit 4 in 2nd case 2b. That is, the signal wave form read from the magnetic head 13 is amplified with the R/W amplifier 7, it is sent to the channel circuit 66, signal amplitude is corrected to suitable magnitude in the channel circuit 66, and coding processing is performed. The signal in the channel circuit 66 is incorporated by GA65, taking the synchronization with a reference signal which is generated in the microcomputer 61. After that, once the signal in GA65 is sent to HDC63 according to directions of a microcomputer 61 and is stored in RAM64, it is transmitted to the information machines and equipment circuit 4 in conformity with an interface bus method." (Emphasis added).

The above description shows that the channel circuit 66 deals with an analog signal. In addition, R/W amplifier 7 also deals with an analog signal. Therefore, the signal between the channel circuit 66 and the R/W amplifier is an analog signal. Thus, there is no analog/digital converter in the circuit board 2a of the Takao et al. reference.

Regarding claim 6, contrary to the Examiner's allegation, the Takao et al. reference does not teach or suggest spindle motor/voice coil motor control circuits 8 (9 and 10) on the second printed circuit board 2b. Rather, the Takao et al. reference only discloses a spindle

Regarding claim 8, the Takao et al. reference discloses:

"In a logic operation circuit 6, the timing clock written as information

to a magnetic disk 11 is generated, and the signal reworked according to the clock is delivered and received between the R/W amplifier 7. Moreover, a logic operation circuit 6 performs transfer of the device section drive circuit 8 and control signal which have been arranged in 1st cast 2a to coincidence, controls migration of rotation of magnetic disk 11 and the magnetic head 13 to it, and makes a necessary truck and a sector move the magnetic head 13 to it."

Therefore, the Takao et al. reference does not teach or suggest a single voice coil motor driver 9 and a single motor driver 10 in the second printed circuit board. There is not a plurality of voice coil motor driver and a plurality of motor drivers in the second printed circuit board.

The Takao et al. reference discloses an interface control circuit 5 and logic calculation circuit 6 in the second printed circuit board. However, the interface control circuit 5 and the logic calculation circuit 6 are function blocks. A circuit block diagram such as Figures 1 and 3 is unable to show a physical structure, and there is no figure showing a separated physical structure of the second printed circuit board. Therefore, in the Takao et al. reference, there is no disclosure of the second printed circuit board separated into a plurality of printed circuit boards, one of which is provided for an interface control circuit 5 and another of which is provided for a logic calculation circuit 6.

Therefore, the Examiner is respectfully requested to withdraw the rejection of claims 1, 3, 5-10, and 12.

III. FORMAL MATTERS AND CONCLUSION

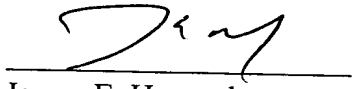
In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1, 3, 5-10, 12, and 14-19, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/7/05



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